Developing Wide Flexible Robust PWM Driver by Flip Flop For Supporting The SMPS Technology

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***Abstract*— The limitation of the operational area of the PWM signal generator provided by the microprocessor or chip, give the opportunity to develop flip flop technology that has been widely used in digital technology as a latch, counter, register, memory and so on, will be able to be developed into a PWM driver. Flip flop technology has developed and is able to reach a very wide operational area regarding voltage and frequency variations. So in this research flip flop technology was developed as a PWM signal driver and the results were better, involving the ability to vary voltage from 6 to 60 Volts, frequencies from 2 to 81 kHz and duty cycles of 10 -75%. Furthermore, if a component with higher capability is selected, it will be able to operate in very low to very high operating areas, exceeding the capabilities of the microprocessor or chip.**

Keywords— flip flop, pwm, smps, duty cycle, switching

I. INTRODUCTION

Signal PWM (pulse width modulation) plays an important role in SMPS (switching mode power supply) technology, namely in the development of converters, inverters or motor control, which presents the transformation of ac - dc electric power and vice versa in varying voltages and currents [1], [2], [3]. Regular PWM generators use microcontrollers or common signal generator chips such as NE555 or special LMM 494 PWM, SSC1S311 chip generators, but have very limited operational areas. Like a microcontroller only operates at 3 to 5 volts and frequency is limited to the type of microcontroller. Also the PWM generator chip also only operates at limited frequency and voltages less than 30 volts.

Power transformation technology need a very wide area range from very low to very high voltage and frequency. Especially the HVDC technology requires digital technology at high voltage and frequency for transmission and distribution of electrical power.

If flip flop technology can be built by components that are able to work in a very wide operational area, then if it can be developed as a PWM driver, then the limited work area of the available PWM driver will get a solution. Then the problem is how to develop the flip flop as a PWM driver is what will be done in this study.

A. Flip-flop technology

The flip-flop circuit is commonly used as a digital component, in the form of logic gates that are widely used as sequential logic in computer devices. It is also a stable multi vibrator that can be used as a stable periodic wave generator. The types of flip flop that are widely used are RS flip flop, D flip flop, JK flip flop, T flip flop [4].

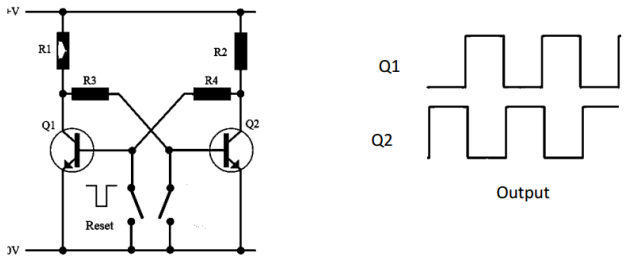

Fig. 1 : Basic circuit of flip-flops

Figure 1 shows the basic circuit of flip-flops, which will be developed to be able to become a flexible flip-flop that is reliable and able to work in large operational areas.

From this basic circuit, flip flop technology has been developed by researchers, as follow :

1. High-speed flip flop technology has been developed up to 113 GHz by S. Trotta et. al [5], explains that: a tunable flip flop-based frequency divider and a fully differential push-push VCO designed in a 200GHz Ft SiGe BiCMOS technology. A new technique for tuning the sensitivity of the divider in the frequency range of interest is presented.
2. Optical technology for flip flops developed by Sanmukh Kaur et. al [6], explains that: a simple and novel scheme for all-optical SR and D flip-flop employing cross gain modulation (XGM) effect in two wideband semiconductor optical amplifiers. The proposed flip-flop has a fast response, with less than 20 ps transition times for both rising and falling edges. The FF speed limit is mainly determined by the SOA recovery time and the intra-FF coupling length.

3. Very low power flip flop technology was developed by Ahmad Karimi, et. al [7] who explained that : The power efficiency and reducing the layout area are two main concerns in D-Flip-Flops (D-FF) design. In this paper, a novel architecture is presented for the pulse-triggered D-FF in the CMOS 90-nm technology. It utilizes a transmission gate for control the input data and the leakage power. The Pulse Generator (PG) is also modified to reduce the number of required transistors and the clock pulse delay. The pull-up P-MOS transistor is also controlled by input data to reduce the power dissipation..
4. High speed and low power flip flop technology has also been developed by M. Prithivi Raj et. al [8] with Dynamic signal driving strategy, explained that : capacity is more important to the synchronous framework, consideration needs to provide for the attributes of these clock signals. In the sequential circuits, a clock distribution system spends a lot of power given the high operating frequency of high capacitance. An existing approach to reducing the limits of a clock signal is based on the quantity of clocked transistors. In this, an advanced procedure is proposed and evaluated by utilizing Dual-Edge Triggered Flip-Flop (DETFF) depends on the Dynamic Signal Driving (DSD) strategy. It is executed in sequential circuits that have been ordered using Tanner Electronic Design Automation (EDA) tool which is used to simulate and examine control by using the Dynamic Signal Driving (DSD) strategy.
5. Flip flop technology with very wide voltage operational areas has also been developed by Sébastien Bernarda et. al [9] proposing that : pulse-triggered flip-flops (pulsed-FF) and register file in 28 nm Ultra-Thin-Body-and Box Fully-Depleted-Silicon-on-Insulator (UTBB-FDSOI) technology, dedicated to ultra-wide voltage range (UWVR) operation. A pulsed-FF composed of a latch and a pulse generator offers potential power performance area (PPA) advantages over the conventional master-slave flip-flop. A comparative study of six different latch topologies, in the energy-delay (E – D) space, points out the most efficient architectures. We demonstrate that the tuning capability based on the wide MOSFET back biasing range available in UTBB-FDSOI allows covering the whole (E – D) space with a single sizing. For the pulse generation, we propose a new delay generator to guarantee the robustness at an ultra-low voltage (ULV), down to 0.35 V. The PPA and robustness improvement of the proposed pulsed-FF are demonstrated by silicon measurements, and its tuning capabilities based on back biasing are discussed.
6. The next flip flop technology is that a reliable flip flop can be developed with multi threshold input by Jing Hua Yang et. al [10] explaining that : describing two single input threshold gate (TLG) designs, which are functionally equivalent to differential flip flops. We present a detailed comparison of TLGs with two well established D-flip flop designs. The comparisons are done in both 65 nm and 28 nm commercial processes. We compare total delay, which is defined as the sum of setup delay and clock to output delay. We also show a comparison of tolerance against noise and process variation between the different designs. The two proposed designs are found to be as robust as an existing D-flip flop from both commercial standard cell libraries.
7. On the basis of multi threshold input, a more dynamic flip flop can be developed by Aminur Rahman et. al [11] who explains that : Chaotic Set Reset (RS) flip-flop circuits are investigated once again in the context of discrete planar dynamical system models of the threshold voltages. But this time starting with simple bilinear component models derived from first principles. The dynamics of the minimal model is described in detail, and shown to exhibit some of the expected properties, but not the chaotic regimes typically found in simulations of physical realizations of chaotic flip-flop circuits. Any electronic physical realization of a chaotic logical circuit must necessarily involve small perturbations from the ideal-usually with large or even nonexistent derivatives in small diameter subsets of the phase space. Therefore, perturbed forms of the minimal model are also analyzed in considerable detail. It is proved that very slightly perturbed minimal models can exhibit chaotic regimes, sometimes associated with chaotic strange attractors, as well as some of the bifurcations present in most of the differential equations models for similar physical circuit realizations.

Based on the development of the flip flop technology, high-speed, low-power, reliable and wide-area, the flip flop can be developed as a good PWM signal driver.

B. PWM technology

There are two types of analog modulation: • continuous analog modulation amplitude modulation (AM); Frequency modulation (FM); Phase modulation (P.M) • Analog modulation with Pulse Amplitude Modulation (PAM) pulses; Pulse Width Modulation (PWM); Pulse Position Modulation (PPM) [12]. PWM is a periodic signal that generates pulse width modulation at certain frequencies and provides DC (duty cycle) or varying effective cycle power.

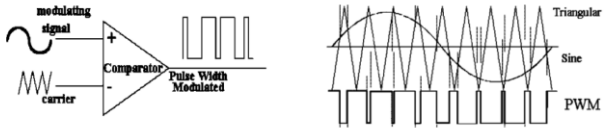

Fig. 2 : Development of PWM signals

Figure 2 explains the formation of a PWM signal when combined with a sine signal with a triangular signal. It can be seen that the life and death times during a period are not the same. If a longer life time will produce a higher voltage output, and vice versa. Comparison of life time with a period of time is called Duty Cycle (DC). DC (duty cycle) is the percentage of effective power in a cycle given the following description :

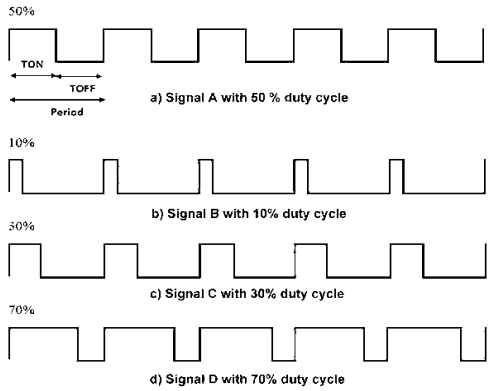

Fig. 3: Duty cycle of various signal forms

$$\text{Duty Cycle} = \frac{T_{on}}{T_{on}+T_{off}} \quad (1)$$

Period = $T_{on} + T_{off}$

Effective power rms given formula (2)

$$P_{rms} = \sqrt{\frac{1}{T}\int_0^T \left(v(t).i(t)\right)^2 .dt} \quad (2)$$

The greater the duty cycle will produce greater effective power and the higher the voltage, conversely if the smaller duty cycle will produce less effective power and the voltage also drops. Thus by providing certain duty cycles, certain voltages can be generated as needed, with very wide variations. This is as developed by Mr. Sanjay Murmu et. al [13] which explains that : DC-DC switching converters are widely used for a sophisticated application. By using these converters with given dc input voltage a stabilized output voltage can be obtained by using Buck (lower), Boost (higher), or Buck-Boost topology which improves the efficiency of the dc-dc converter as compared to linear regulators. The most used technique for control switching power supply is PWM. In this way, a particular dc-dc converter is designed by keeping the typical application. A properly designed dc-dc converter provides many advantages such as low ripple, better noise rejection, reliable and efficient converter. For some typical applications like powering LED, it needs constant current supply for constant illumination. Hence the feedback based closed-loop converters become a better choice. In the present thesis for low power application, a PWM based closed-loop dc-dc buck converter has been designed, analyzed, and simulated. A MOSFET has been used as a switching device and components have been designed for low ripple and low noise. With variation in load and variation in input power supply output supply voltage has been obtained as constant value by using a PID controller. The performance of the PID controller and switching frequency have been adjusted such that the output voltage maintain at 8 V.

C. Switching technology

Switching technology is a new technology in the electronic system that allows the digital voltage and current regulation, which is referred to as SMPS (switching mode power supply) technology. Electric power sources are usually channeled using MOSFETs or IGBT with large power, the distribution pattern is regulated by the PWM generator as a trigger.

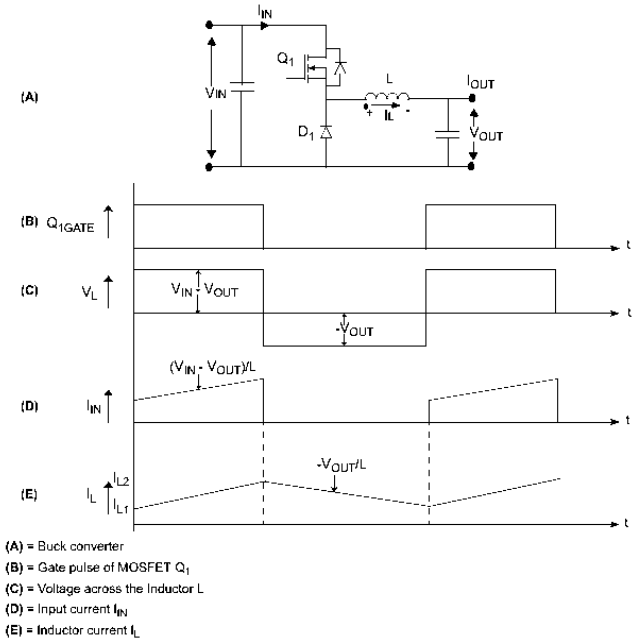

Fig. 4 : Switching system technology [14]

Figure 4 shows a switching system for managing electricity from source to equipment, which is able to adjust the needs of the equipment that uses it. This circuit is often referred to as a buck-boost converter, which transforms ac or dc to dc or ac power sources with various voltages as needed. This can work with PWM signal generator settings.

II. FIP FLOP DEVELOPMENT

The development of a capable flip flop that can operate in wide operational areas based on variations in voltage, frequency and duty cycle is as follows :

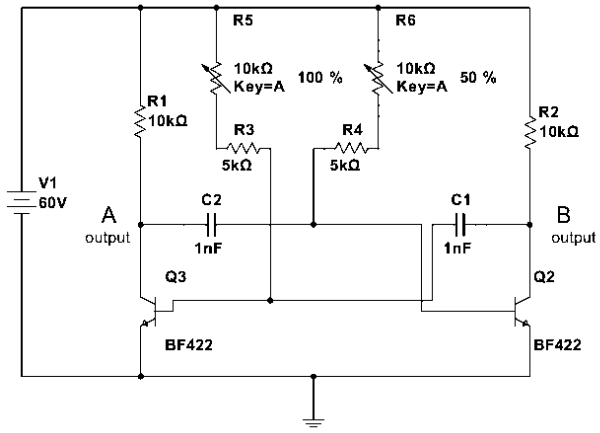

Fig. 5 : Development of a flip flop as a PWM signal driver

Figure 5 is the development of the flip flop as a PWM signal driver, which will produce a PWM signal at output A or B. The trim port positions of R5 and R6 as initial

resistance that provide voltage threshold will determine the frequency and duty cycle.

III. Results and Discussion

Based on the flip flop design in Figure 5, a variable power source is installed which can be changed to 60 Volts or more depending on the type of transistor used. The PWM signal generated at the output is seen with an oscilloscope, as shown in the following figure:

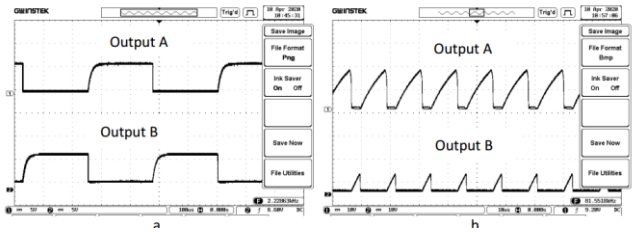

Fig. 6: Low and high frequency flip flop output signals

Figure 6.a shows the PWM signal output flip flop for low frequency 2.2 kHz with a source voltage of 6 volts. Figure 6.b shows the PWM signal output flip flop for a low frequency of 81.2 kHz with a source voltage of 36 volts.

The output signal results from experiments with various threshold voltage settings performed with the initial trigger resistance setting, is given in the next figure.

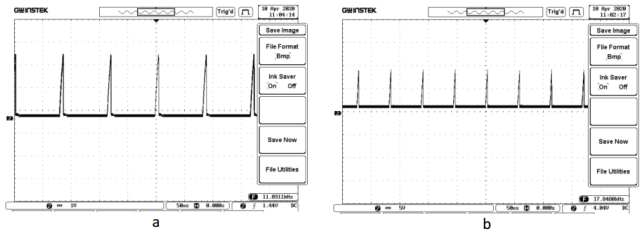

Fig. 7 : PWM signal output with DC 10%

Figure 7 shows the results of a PWM signal with a duty cycle of around 10%, 7.a at a frequency of 11.0 kHz, 7.b at a frequency of 17.8 kHz.

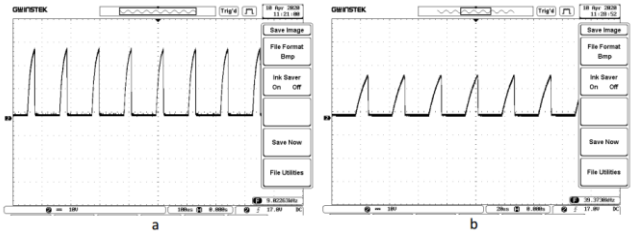

Fig. 8 : PWM signal output with DC 25 %

Figure 8 shows the results of a PWM signal with a duty cycle of around 25 %, 8.a at a frequency of 9.0 kHz, 8.b at a frequency of 39,3 kHz.

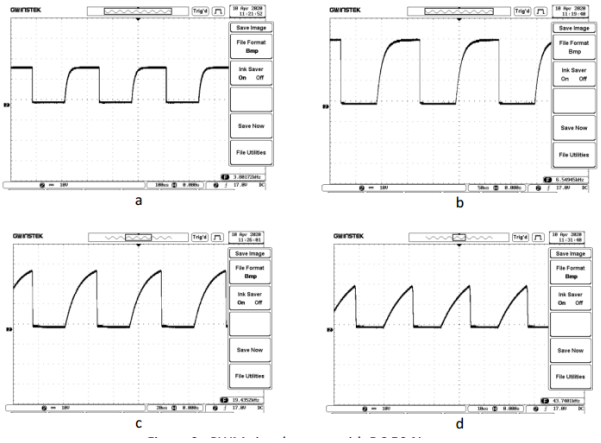

Fig. 9 : PWM signal output with DC 50 %

Figure 9 shows the results of a PWM signal with a duty cycle of about 50%, 7.a at a frequency of 3 kHz, 9.b at a frequency of 6.5 kHz, 9.c at a frequency of 19.4 kHz, 9.d at a frequency of 43.7 kHz

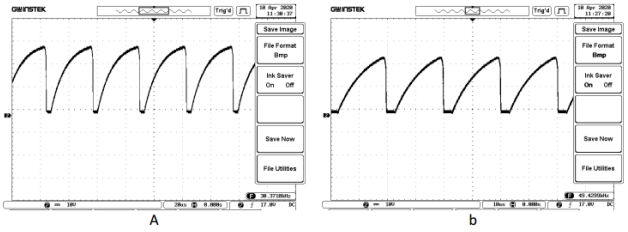

Fig. 10 : PWM signal output with DC 60 %

Figure 10 shows the results of a PWM signal with a duty cycle of around 60 %, 10.a at a frequency of 37,3 kHz, 10.b at a frequency of 39,4 kHz.

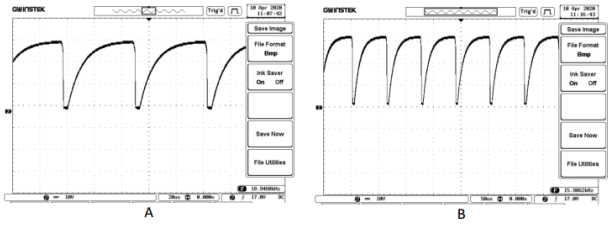

Fig. 11 : PWM signal output with DC 75 %

Figure 11 shows the results of a PWM signal with a duty cycle of around 75 %, 11.a at a frequency of 10,9 kHz, 11.b at a frequency of 15,9 kHz.

IV. Conclusions

The development of the flip flop is equipped with initial resistance as threshold voltage, PWM signal drives with various and reliable of voltage, duty cycles and frequencies can be produced by various operating areas well. It has been successfully developed with in voltage : 6-60 V0lt, frequencies : 2-81 kHz and duty cycle (DC) : 10- 75%. This means that the development of the flip flop can be used as a signal driver for developing flexible and robust SMPS technology.

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